Curriculum Vitae

Bharat L. Bhuva
Professor
Department of Electrical Engineering and Computer Science
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Education:

- Ph.D., Electrical Engineering, North Carolina State University, Raleigh, NC, December 1987
- M.S., Electrical Engineering, North Carolina State University, Raleigh, NC, May, 1984
- B.E., Electronics Engineering, M. S. University of Baroda, Baroda, India, July, 1982

Professional Experience:

9/87 – Present: Professor, Associate Professor, and Assistant Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science
Vanderbilt University

2008 – 2012: Director of Graduate Studies
Department of Electrical Engineering and Computer Science
Vanderbilt University

1993 – 1998: Associate Director
University Consortium for Research on Electronics in Space
Department of Electrical and Computer Engineering
Vanderbilt University

1984-1987: Design Engineer
Microelectronics Center of North Carolina
Research Triangle Park, NC 27910

1984-1987: Research Assistant
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27695

1982-1984: Teaching Assistant
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27695

Summer 1981: Summer Trainee
Air India
Santa Cruz, India

Honors and Awards:

Best Paper Award at the 2012 Chips at Cisco Conference
Best Poster Paper Award at the 2011 IEEE International Reliability Physics Symposium
Best Paper Award at the 2010 Government Microcircuit Applications and Critical Technology Conference
Best Paper Award at the 2007 European Conference on Radiation and Its Effects on Components and Systems
Best Paper Award at the 2007 Government Microcircuit Applications and Critical Technology Conference.
Finalist for The Best Paper award at 2005, 2006, 2007, 2008, 2009, 2011, 2012, 2013, 2014 IEEE Nuclear and Space Radiation Effects Conference.
Best Student Paper Award at the 2012 IEEE Nuclear and Space Radiation Effects Conference.
Best Student Paper Award for the School of Engineering, Vanderbilt University, 2007.
Best Student Paper Award at the 2006 IEEE Nuclear and Space Radiation Effects Conference.
Best Student Paper award at the 2005 European Conference on Radiation and Its Effects on Components and Systems.
Finalists for The Best Student Paper award at 2007, 2008, 2009, 2013 IEEE Nuclear and Space Radiation Effects Conference.
President of the Graduate Student Association, ECE Department, NCSU, 1986-1987.
Vice-President of the Graduate Student Association, ECE Department, NCSU, 1986-1987.
Presidents Scholar, 1976 (Award is given to students scoring highest marks in post secondary exam).

Research Interests:

Professor Bhuva's current research interests are in microelectronics and bio-sensors. His group is involved in characterizing effects of radiation on semiconductor circuits, devices, and materials at the most advanced technology nodes. He has developed circuit simulators for failure identification, mitigation, and performance estimation. His work on single-event transient vulnerability has been used widely by the industry. His work on soft error mitigation has received numerous awards. His research group was the first to measure (i) pico-seconds long single-event transient pulses (this circuit design has been used by most semiconductor companies for SET characterization), (ii) charge collected by a node due to a single-event strike, and (iii) parasitic bipolar characteristics after a single-event strike for advanced CMOS technologies. He is also active in the area of bio-sensor technology development where advances in the area of electrical engineering and biochemistry were combined to develop highly sensitive and selective bio-sensors based on conventional CMOS fabrication process. Another area of his research is optical interconnects for ICs. His group has demonstrated reverse-biased optical operation of p-n junctions at 10's of GHz range frequencies along with models for light emission and reliability of optical emitters. This work has been used to demonstrate intra- and inter-chip optical interconnects entirely based on conventional Si-based CMOS fabrication process. He has also worked in the oxide reliability area where his group developed techniques and models for accelerating the aging process for CMOS devices. The technique was widely adopted by semiconductor manufacturers for evaluating gate insulators.

Research Funding:

Research funding from sources that include NSF, DTRA, NRO, DARPA, ONR, AFOSR, SRC, and semiconductor companies including Altera, AMD, Avago, ARM, Boeing, Broadcom, Cisco Systems, Freescale, LSI Logic, Marvell, MediaTek, Qualcomm, Renesas, Synopsys, TSMC, and Xilinx. He has also received funding continuously since 2007 from Silicon Valley Community Foundation. Total funding as PI and Co-PI is in excess of $35 Million since 1987.

Current Research Funding (as PI, Co-PI, or Investigator) (Career funding in excess of $35M) :

- Silicon Valley Community Foundation
  Logic Designs for In-Field Repair and Failure Mitigation
  Total Budget: $60,000
  Contract Period: 12/11 – 7/14

- Robust Chip / DTRA
  Solutions for Single-Event Error in Ultra Deep Submicron Semiconductor Technologies Using Simulation
  Total Budget: $259,885
  Contract Period: 8/12 – 8/2014

- Silicon Valley Community Foundation
  Effects of X-ray based PCB Inspection Systems on Transistor Parameters
  Total Budget: $60,000
  Contract Period: 8/13 – 7/14

- Aero Thermo / Navy
  SSP D5LE Program Support
  Total Budget: $1,310,190
  Contract Period: 1/13 – 12/15

- NRO
  Radiation Hardened Nano-Scale Integrated Circuits Microelectronics Technology
  Total Budget: $298,407
  Contract Period: 8/13 – 2/15

- DTRA
  Characterization and Mitigation of Nanoscale CMOS
  Total Budget: $2,500,175
  Contract Period: 8/13 – 7/16

- NRL
  Study of Total Ionizing Dose Radiation Effects in FinFET CMOS Technologies
  Total Budget: $200,594
  Contract Period: 10/13 – 9/16

- TSMC Soft Error Industry Coalition (Altera, AMD, ARM, Avago, Broadcom, Cisco Systems, LSI Logic, Marvell, MediaTek, Qualcomm, Renesas, Synopsys, and TSMC)
  Soft Error Evaluation of 16-nm Technology Node
  Total Budget: $1,298,595
  Contract Period: 3/14 – 2/17

- NRO
  Radiation Mitigation in Disruptive Nanoscale Technologies
  Total Budget: 449,586
  Contract Period: 8/2014 – 7/2017

Journal Publications: (h-index of 30 and i-10 index of 86, total citations over 3100)

1. I. Chatterjee, E. X. Zhang, B. L. Bhuva, R. Reed, M. L. Alles, D. Ball, R. D. Schrimpf, D. M. Fleetwood, D. Linten, E. Simoen, C. Claeys, "Geometry Dependence of Total-Dose Effects in Bulk FinFETs," IEEE Transactions on Nuclear Science, Vol. 61, No. 6, pp. 2951-2958, December 2014.
2. Y. P. Chen, T. D. Loveless, P. Maillard, N. J. Gaspard, S. Jagannathan A. F. Witulski, B. L. Bhuva, W. T. Holman, and L. W. Massengill, "Quantification of Single-Event Harmonic Errors in Ring Oscillators," IEEE Transactions on Nuclear Science, Vol. 61, No. 6, pp. 3163-3170, December 2014.
3. N. N. Mahatme, N. J. Gaspard, T. Assis, T. D. Loveless, B.L. Bhuva, W. H. Robinson, L. W. Massengill, S.-J. Wen, and R. Wong, "Power-Aware Mitigation of Combinational Logic Soft Errors," IEEE Transactions on Nuclear Science, Vol. 61, No. 6, pp. 3274-3281, December 2014.
4. Y. Ren, A.-L. He, S.-T. Shi, G. Guo, L. Chen, S.-J. Wen, R. Wong, N. W. VanVonno, and B. L. Bhuva, "Single-Event Transient Measurements on a DC/DC Pulse Width Modulator Using Heavy Ion, Proton, and Pulsed Laser," Journal of Electronic Testing, Vol. 30, No. 1, pp. 149-154, February 2014.
5. I. Chatterjee, B. Bhuva, R. Reed, R. Schrimpf, B. Narasimham, J. K. Wang, N. Vedula, B. Bartz, C. Monzel, "Impact of Technology Scaling on SRAM Soft Error Rates," IEEE Transactions on Nuclear Science, Vol. 61, No. 6, pp. 3512-3518, December 2014.
6. N. N. Mahatme, N. J. Gaspard, S. Jagannathan, T. D. Loveless, I. Chatterjee, B. L. Bhuva, L. W. Massengill, R. D. Schrimpf, "Experimental Estimation of the Window of Vulnerability for Logic Circuits," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 4, Pp. 2691 – 2696, 2013.
7. D. B. Limbrick, N. N. Mahatme, W. H. Robinson, B. L. Bhuva, "Reliability-Aware Synthesis of Combinational Logic With Minimal Performance Penalty," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 4, Pp. 2776 – 2781, 2013.
8. K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, D. Loveless, B. Bhuva, "Single-Event Performance and Layout Optimization of Flip-Flops in a 28-nm Bulk Technology," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 4, Pp. 2782 – 2788, 2013.
9. Z. J. Diggins, N. J. Gaspard, N. N. Mahatme, S. Jagannathan, T. D. Loveless, T. R. Reece, B. L. Bhuva, A. F. Witulski, L. W. Massengill, S.-J. Wen, R. Wong, "Scalability of Capacitive Hardening for Flip-Flops in Advanced Technology Nodes," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
10. N. J. Gaspard, S. Jagannathan, Z. J. Diggins, M. P. King, S.-J. Wen, R. Wong, T. D. Loveless, K. Lilja, M. Bounasser, T. Reece, A. F. Witulski, W. T. Holman, B. L. Bhuva, L. W. Massengill, "Technology Scaling Comparison of Flip-Flop Heavy-Ion Single-Event Upset Cross Sections," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
11. S. Guo, J. Li, P. Gui, Y. Ren, L. Chen, B. L. Bhuva, "Single-Event Transient Effect on a Self-Biased Ring-Oscillator PLL and an LC PLL Fabricated in SOS Technology," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
12. N. M. Atkinson, W. T. Holman, J. S. Kauppila, T. D. Loveless, N. C. Hooten, A. F. Witulski, B. L. Bhuva, L. W. Massengill, E. X. Zhang, J. H. Warner, "The Quad-Path Hardening Technique for Switched-Capacitor Circuits," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
13. J. A. Maharrey, R. C. Quinn, T. D. Loveless, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. X. Zhang, M. L. Alles, B. L. Bhuva, W. T. Holman, L. W. Massengill, "Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
14. I. Chatterjee, E. X. Zhang, B. L. Bhuva, M. L. Alles, R. D. Schrimpf, D. M. Fleetwood, Y.-P. Fang, A. Oates, "Bias Dependence of Total-Dose Effects in Bulk FinFETs," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
15. N. N. Mahatme, N. J. Gaspard, S. Jagannathan, T. D. Loveless, B. L. Bhuva, W. H. Robinson, L. W. Massengill, S.-J. Wen, R. Wong, "Impact of Supply Voltage and Frequency on the Soft Error Rate of Logic Circuits," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
16. S. Jagannathan, T. D. Loveless, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, T. D. Haeffner, J. S. Kauppila, N. N. Mahatme, B. L. Bhuva, M. L. Alles, W. T. Holman, A. F. Witulski, L. W. Massengill, " Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation," IEEE Trans. on Nucl. Sci., Volume 60 , Issue 6, December 2013.
17. Y. Ren, L. Fan, L. Chen, S.-J. Wen, R. Wong, N. W. van Vonno, A. F. Witulski, B. L. Bhuva, "Single-Event Effects Analysis of a Pulse Width Modulator IC in a DC/DC Converter," Journal of Electronic

Testing, Volume 28, Issue 6, pp 877-883, December 2012
18. N. A. Dodds, N. C. Hooten, R. A. Reed, R. D. Schrimpf, J. H. Warner, N. J.-H. Roche, D. McMorrow, S.-J. Wen, R. Wong, J. F. Salzman, S. Jordan, J. A. Pellish, C. J. Marshall, N. J. Gaspard, W. G. Bennett, E. X. Zhang, B. L. Bhuva, "Effectiveness of SEL Hardening Strategies and the Latchup Domino Effect," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2642 - 2650, December 2012
19. A. V. Kauppila, B. L. Bhuva, T. D. Loveless, S. Jagannathan, N. J. Gaspard, J. S. Kauppila, L. W. Massengill, S. J. Wen, R. Wong, G. L. Vaughn, W. T. Holman, " Effect of Negative Bias Temperature Instability on the Single Event Upset Response of 40 nm Flip-Flops," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2651 - 2657, December 2012
20. J. S. Kauppila, S. Jagannathan, D. R. Ball, J. D. Rowe, N. J. Gaspard, N. M. Atkinson, R. W. Blaine, T. R. Reece, J. R. Ahlbin, T. D. Haeffner, M. L. Alles, W. T. Holman, B. L. Bhuva, L. W. Massengill, T. D. Loveless, "On-Chip Measurement of Single-Event Transients in a 45 nm Silicon-on-Insulator Technology," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2748 - 2755, December 2012
21. S. Jagannathan, T. D. Loveless, B. L. Bhuva, N. J. Gaspard, N. N. Mahatme, T. Assis, S.-J. Wen, R. Wong, L. W. Massengill, "Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40-nm CMOS Technology," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2796 - 2802, December 2012
22. B. Narasimham, K. Chandrasekharan, Z. Liu, J. K. Wang, G. Djaja, N. J. Gaspard, J. S. Kauppila, B. L. Bhuva, "A Hysteresis-Based D-Flip-Flop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2847 - 2851, December 2012
23. N. N. Mahatme, E. X. Zhang, R. A. Reed, B. L. Bhuva, R. D. Schrimpf, D. M. Fleetwood, D. Linten, E. Simoen, A. Griffoni, M. Aoulaiche, M. Jurczak, G. Groeseneken, "Impact of Back-Gate Bias and Device Geometry on the Total Ionizing Dose Response of 1-Transistor Floating Body RAMs," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 6 , Part: 1, Page(s): 2966 – 2973, December 2012
24. N. N. Mahatme, B. L. Bhuva, Y.-P. Fang, A. S. Oates, "Impact of Strained-Si PMOS Transistors on SRAM Soft Error Rates," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 4 , Part: 1, Page(s): 845 - 850, June 2012
25. I. Chatterjee, B. L. Bhuva, S.-J. Wen, R. Wong, "Influence of User-Controlled Parameters in Alpha Particle-Induced Single-Event Error Rates in Commercial SRAM Cells," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 4 , Part: 1, Page(s): 872 - 879, June 2012
26. A. V. Kauppila, D. R. Ball, B. L. Bhuva, L. W. Massengill, W. T. Holman, "Impact of Process Variations on Upset Reversal in a 65 nm Flip-Flop," IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 4 , Part: 1, Page(s): 886 - 892, June 2012
27. D. Rennie, D. Li, M. Sachdev, B.L. Bhuva, S. Jagannathan, Shi-Jie Wen, R. Wong, "Performance, Metastability, and Soft-Error Robustness Trade-offs for Flip-Flops in 40 nm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 59 , Issue: 8, Page(s): 1626 – 1634, 2012
28. M. J. Gadlage, J. R. Ahlbin, B. Narasimham, B. L. Bhuva, L. W. Massengill, R. D. Schrimpf, Single-Event Transient Measurements in nMOS and pMOS Transistors in a 65-nm Bulk CMOS Technology at Elevated Temperatures," IEEE Trans. On Materials and Device Reliability, Vol. 11, No. 1, pp. 179-186, 2011.
29. J. R. Ahlbin, M. J. Gadlage, N. M. Atkinson, B. Narasimham, B. L. Bhuva, A. F. Witulski, W. T. Holman, P. H. Eaton, L. W. Massengill, Effect of Multiple-Transistor Charge Collection on Single-Event Transient Pulse Widths," IEEE Trans. On Materials and Device Reliability, Vol. 11, No. 3, pp. 401-406, 2011.
30. A. V. Kauppila, B. L. Bhuva, J. S. Kauppila, L. W. Massengill, W. T. Holman, Impact of Process Variations on SRAM Single Event Upsets," IEEE Trans. On Nuclear Science, Vol. 58, No. 3, pp. 843-839, June 2011.
31. M. J. Gadlage, J. R. Ahlbin, B. L. Bhuva, N. C. Hooten, N. A. Dodds, R. A. Reed, L. W. Massengill, R. D. Schrimpf, G. Vizkelethy, " Alpha-Particle and Focused-Ion-Beam-Induced Single-Event Transient Measurements in a Bulk 65-nm CMOS Technology," IEEE Trans. On Nuclear Science, Vol. 58, No. 3, pp. 1093-1097, June 2011.
32. N. M. Atkinson, A. F. Witulski, W. T. Holman, J. R. Ahlbin, B. L. Bhuva, L. W. Massengill, " Layout Technique for Single-Event Transient Mitigation via Pulse Quenching," IEEE Trans. On Nuclear Science, Vol. 58, No. 3, pp. 885-890, June 2011.
33. T. D. Loveless, S. Jagannathan, T. Reece, J. Chetia, B. L. Bhuva, M. W. McCurdy, L.W. Massengill, S.-J. Wen, R. Wong, D. Rennie, " Neutron- and Proton-Induced Single Event Upsets for D- and DICE-Flip/Flop

Designs at a 40 nm Technology Node," IEEE Trans. On Nuclear Science, Vol. 58, No. 3, pp. 1008-1014, June 2011.
34. N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, B. L. Bhuva, T. D. Loveless, L. W. Massengill, "Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2614-2620, December 2011.
35. N. M. Atkinson, J. R. Ahlbin, A. F. Witulski, N. J. Gaspard, W. T. Holman, B. L. Bhuva, E. X. Zhang, L. Chen, L. W. Massengill, " Effect of Transistor Density and Charge Sharing on Single-Event Transients in 90-nm Bulk CMOS," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2578-2584, December 2011.
36. A. V. Kauppila, B. L. Bhuva, L. W. Massengill, W. T. Holman, D. R. Ball, "Impact of Process Variations and Charge Sharing on the Single-Event-Upset Response of Flip-Flops," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2658-1663, December 2011.
37. J. R. Ahlbin, N. M. Atkinson, M. J. Gadlage, N. J. Gaspard, B. L. Bhuva, T. D. Loveless, E. X. Zhang, L. Chen, L. W. Massengill, " Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2585-2590, December 2011.
38. J. S. Kauppila, T. D. Haeffner, D. R. Ball, A. V. Kauppila, T. D. Loveless, S. Jagannathan, A. L. Sternberg, B. L. Bhuva, L. W. Massengill, " Circuit-Level Layout-Aware Single-Event Sensitive-Area Analysis of 40-nm Bulk CMOS Flip-Flops Using Compact Modeling," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2680-2686, December 2011.
39. S. Jagannathan, T. D. Loveless, B. L. Bhuva, S.-J. Wen, R. Wong, M. Sachdev, D. Rennie, L. W. Massengill, "Single-Event Tolerant Flip-Flop Design in 40-nm Bulk CMOS Technology," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 3033-3037, December 2011.
40. N. N. Mahatme, S. Jagannathan, T. D. Loveless, L. W. Massengill, B. L. Bhuva, S.-J. Wen, R. Wong, "Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2719-2725, December 2011.
41. I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. D. Schrimpf, J. K. Wang, B. Bartz, E. Pitta, M. Buer, "Single-Event Charge Collection and Upset in 40-nm Dual- and Triple-Well Bulk CMOS SRAMs," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2761-2767, December 2011.
42. P. M. Gouker, B. Tyrrell, M. Renzi, C. Chen, P. Wyatt, J. R. Ahlbin, S. Weeden-Wright, N. M. Atkinson, N. J. Gaspard, B. L. Bhuva, L. W. Massengill, E. X. Zhang, R. D. Schrimpf, R. A. Weller, M. P. King, M. J. Gadlage, "SET Characterization in Logic Circuits Fabricated in a 3DIC Technology," IEEE Trans. On Nuclear Science, Vol. 58, No. 6, pp. 2555-2562, December 2011.
43. M. J. Gadlage, J. R. Ahlbin, B. Narasimham, B. L. Bhuva, L.W. Massengill, R. A. Reed, R. D. Schrimpf, and G. Vizkelethy, "Scaling trends in SET pulse widths in sub-100 nm bulk CMOS processes," IEEE Transactions on Nuclear Science, Vol. 57, No. 6, PP. 3336-3341, December 2010
44. P. Maillard, W. T. Holman, T. D. Loveless, B. L. Bhuva, L. W. Massengill, "An RHBD technique to mitigate missing pulses in delay locked loops," IEEE Transactions on Nuclear Science, Vol. 57, No. 6, PP. 3634-3639, December 2010.
45. S. Jagannathan, M. J. Gadlage, B. L. Bhuva, R. D. Schrimpf, B. Narasimham, J. Chetia, J. R. Ahlbin, and L. W. Massengill, "Independnt measurement of SET pulse widths from N-hts and P-hits in 65 nm CMOS," IEEE Transactions on Nuclear Science, Vol. 57, No. 6, PP. 3386-3391, December 2010.
46. J. R. Ahlbin, M. J. Gadlage, D. R. Ball, A. W. Witulski, B. L. Bhuva, R. A. Reed, G. Vizkelethy, and L. W. Massengill, "The effect of layout topology on single-event transient pulse quenching in a 65 nm bulk CMOS process," IEEE Transactions on Nuclear Science, Vol. 57, No. 6, PP. 3380-3385, December 2010.
47. T. Wang, K. Wang, L. Chen, A. Dinh, B. L. Bhuva, R. L. Shuler, "A RHBD LC-tank oscillator design tolerant to single-event transients," IEEE Transactions on Nuclear Science, Vol. 57, No. 6, PP. 3620-3625, December 2010.
48. T. D. Loveless, L. W. Massengill, W. T. Holman, B. L. Bhuva, D. McMorrow, and J. H. Warner, "A generalized linear model for single event transient propagation j phase-locked loops," IEEE Transactions on Nuclear Science, Vol. 57, No. 5, pp. 2933-2947, October 2010
49. M. J. Gadlage, J. R. Ahlbin, B. Narasimham, V. Ramachandran, C. A. Dinkins, N. D. Pate, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, R. L. Shuler, and D. McMorrow, "Increased single-event transient pulsewidths in a 90-nm bulk CMOS technology operating at elevated temparatures," IEEE Transactions on Device and Materials Reliability, Vol. 10, No. 1, PP. 157-163, March 2010.
50. V. Ramachandran, M. J. Gadlage, J. R. Ahlbin, B. Narasimham, M. L. Alles, R. A. Reed, B. L. Bhuva, L. W. Massengill, J. D. Black, and C. N. Foster, "Application of a Novel Test System to Characterize Single-Event Effects at Cryogenic Temperatures," Solid-State Elect., vol. 54, no. 10, pp. 1052-1059, Oct 2010.

51. M. J. Gadlage, R. D. Schrimpf, B. Narasimham, R. A. Reed, R. A. Weller, and B. L. Bhuva, "Neutron-induced digital single event transient vulnerability of an advanced CMOS process in a nuclear burst environment," The Journal of Radiation Effects: Research and Engineering, Volume 27, Number 1, pp. 87-92, July 2010.
52. M. C. Casey, P. R. Fleming, B. L. Bhuva, J. D. Black, and L. W. Massengill, "HBD using dual redundant circuits and cascode-voltage switch logic gates for SET tolerant digital designs," The Journal of Radiation Effects: Research and Engineering, July 2010.
53. J. R. Ahlbin, L. W. Massengill, B. L. Bhuva, B. Narasimham, M. J. Gadlage, and P. H. Eaton, "Single-event transient pulse quenching in advanced CMOS logic circuits," IEEE Transactions on Nuclear Science, Vol. 56, No. 6, pp. 3050-3056, December 2009
54. T. Wang, L. Chen, A. Dinh, B. L. Bhuva, "Single-event transient effects on dynamic comparators in a 90 nm CMOS triple-well and dual-well technology," IEEE Transactions on Nuclear Science, Vol. 56, No. 6, pp. 3556-3560, December 2009.
55. M.C. Casey, S.E. Armstrong, R. Arora, M.P. King, J.R. Ahlbin, S.A. Francis, B.L. Bhuva, D. McMorrow, H.L. Hughes, P.J. McMarr, J.S. Melinger, L.W. Massengill, "Effect of total ionizing dose on a bulk 130 nm ring oscillator operating at ultra-low power," IEEE Transactions on Nuclear Science, Vol. 56, No. 6, pp. 3262-3266, December 2009.
56. M.J. Gadlage, P. Giuker, B. L. Bhuva, B. Narasimham, and R, D, Schrimpf, "Heavy-ion-induced digital single-event transients in a 180 nm fully-depleted SOI process," IEEE Transactions on Nuclear Science, Vol. 56, No. 6, pp. 3483-3488, December 2009.
57. T.D. Loveless, B.D. Olson, B.L. Bhuva, W.T. Holman, C.C. Hafer, L.W. Massengill, "Analysis of single-event transients in integer-n frequency dividers and hardness assurance implications for phase-locked loops," IEEE Transactions on Nuclear Science, Vol. 56, No. 6, pp. 3489-3498, December 2009
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227. A. Balasubramanian, B. L. Bhuva, R. Mernaugh, and F. Haselton, "Si-based sensor for biological virus detection," Presented at the 2003 IEEE Sensors Conference, Toronto, Canada, September 2003
228. P. Mongkolkachit, B. L. Bhuva, Y. Boulghassoul, J. Rowe, and L. W. Massengill , "Mitigation of single-event transients in CMOS digital circuits," Presented at the 2003 European Conference on Radiation Effects on Components and Systems, Amsterdam, September 2003
229. S. Aghara, R.J. Fink, W.S. Charlton, B. L. Bhuva, M.R. Samadi, J.A. Ochoa, and J.R. Porter, "Degradation of commercially available DAC ICs in mixed-radiation environment," Presented at the 2003 IEEE Nuclear and Space Radiation Effects Conference, Monterey, CA, July 2003
230. A. Chatterjee and B. L. Bhuva, "High speed, high reliability Si-based light emitters for optical interconnects," Presented at the 2002 IEEE International Interconnect Technology Conference, Burlingame, CA, June 2002.
231. A. Chatterjee, B. L. Bhuva, and W. C. Cieslik, "High speed CMOS - Si light emitters for on-chip optical interconnect," Presented at the 2002 Photonics Symposium, Santa Clara, CA, January 2002.
232. X. Zhu, B. L. Bhuva, C. R. Cirba, L. W. Massengill, S. Buchner, and P. Dodd, "A methodology for identifying laser parameters for equivalent heavy-ion hit," Presented at the 2001 IEEE Nuclear and Space Radiation Effects Conference, Vancouver, Canada, July 2001.
233. A. Verma, A. Chatterjee, B. L. Bhuva, and E. Duco Jansen, "All Si-based optical interconnect for signal transmission," Presented at the 2001 IEEE International Interconnect Technology Conference, Burlingame, CA, June 2001.
234. A. Chatterjee, A. Verma, B. L. Bhuva, E. Duco Jansen, and W. C. Lin, "Accelerated stressing and degradation mechanisms for Si-based photo-emitters," Presented at the 2001 IEEE International Reliability Physics Symposium, Orlando, FL, May 2001

235. A.E. Baranski, L. W. Massengill, D.O. van Nort, and B. L. Bhuva, "Single-event faults in combinational logic modeling vulnerability during VHDL design," Presented at the 2000 Topical Research Conference on Reliability, Stanford, CA, October 2000.
236. A. Chatterjee, B. L. Bhuva, D. Jiang, J. Stankus, D. V. Kerns, Jr., and S.E. Kerns, "Feasibility study for Si-based optical VLSI interconnects," Presented at the 2000 Semiconductor Research Corporation TechCon Conference, Phoenix, AZ, September 2000.
237. B. L. Bhuva, D. Jiang, D. V. Kerns, Jr., and S. E. Kerns, "Design and process issues affecting performance of optical interconnects on ICs," Presented at the 2000 Conference on Process Integration and Device Technology, Santa Clara, September 2000.
238. J. K. Shreedhara, H. J. Barnaby, B. L. Bhuva, A. Raparla, D. V. Kerns, Jr., and S. E. Kerns, "Circuit technique for threshold voltage stabilization using substrate bias in total dose environments," Presented at the 2000 IEEE Nuclear and Space Radiation Effects Conference, Reno, NC, July 2000.
239. L. W. Massengill, A. E. Baranski, D. Van Nort, J. Meng, and B. L. Bhuva, "Analysis of single-event upsets at the VHDL design level simulation of the AM2901 bitslice processor," Presented at the 2000 IEEE Nuclear and Space Radiation Effects Conference, Reno, NC, July 2000.
240. D. Jiang, B. L. Bhuva, D. V. Kerns, Jr., and S. E. Kerns, "Comparative analysis of metal and optical interconnect technology," Presented at the 2000 IEEE International Interconnect Technology Conference, Santa Clara, CA, May 2000.
241. M. N. Jaafar Ali, B. L. Bhuva, S. E. Kerns, M. Maher, R. Lawrence, and A. Hoffmann, "Characterizing effects of radiation on forward and reverse saturation characteristics of N-channel devices," Presented at the 1999 European Conference on Radiation Effects on Components and Systems, Fontevraud, France, November 1999
242. P. Mongkolkachit, B. L. Bhuva, S. Prasad, N. Bui, and S. E. Kerns, "Ultra-thin gate oxide degradation under different rates of charge injection," Presented at the 1999 International Microelectronics Manufacturing, Yield, and Reliability Conference, Santa Clara, CA, November 1999
243. S. E. Kerns, D. V. Kerns, D. Jiang, M. de la Bardonnie, P. Mialhe, A. Hoffmann, J.-P. Charles, and B. L. Bhuva, "Optical evidence of damage localization in irradiated and hot-carrier-stressed BJTs," Presented at the 1999 IEEE Nuclear and Space Radiation Effects Conference, Norfolk, VA, July 1999.
244. S. E. Kerns, D. Jiang, M. de la Bardonnie, F. Pelanchon, H. Barnaby, D. V. Kerns, Jr., R. D. Schrimpf, B. L. Bhuva, P. Mialhe, A. Hoffmann, and J.-P. Charles, "Light emission studies of total dose and hot-carrier effects on Silicon junctions," Presented at the 1999 IEEE Nuclear and Space Radiation Effects Conference, Norfolk, VA, July 1999.
245. J. Meng, L. W. Massengill, and B. L. Bhuva, "Single-event upset simulation in CMOS combinational circuit," Presented at the 1999 IEEE Nuclear and Space Radiation Effects Conference, Norfolk, VA, July 1999.
246. B. L. Bhuva, P. Mongkolkachit, N. Bui, and S. E. Kerns, "A study of effects of plasma-induced charging damage on hot-carrier lifetime using pre-stressed data," Presented at the 1999 International Symposium on Plasma Process-Induced Damage, Monterey, CA, May 1999
247. M. Oner, B. L. Bhuva, P. Sisterhen, H. Hasan, and S. E. Kerns, "Simulation of charging voltages on a wafer during plasma etch," Presented at the 1998 International Conference on Microelectronic Manufacturing Yield, Reliability, and Failure Analysis, Santa Clara, CA, September, 1998.
248. M. Oner, V. Janapaty, N. Bui, B. L. Bhuva, and S. E. Kerns, "Effects of magnetic fields in the plasma chamber on hot-carrier response of CMOS devices," Presented at the 1998 International Symposium on Plasma Process-Induced Damage, Honolulu, Hawaii, June 1998.
249. B. L. Bhuva, and S. E. Kerns, "Circuit-level statistical simulation of hot-carrier effects," Presented at the 1997 Semiconductor Research Corporation TRC Conference, Nashville, TN November 1997.
250. T. Balac, S. Brophy, G. Biswas, D. Schwartz, B. L. Bhuva, and J. Bransford, "Cognitive modeling of student understanding of basic electrical concept," Presented at the 1997 Conference on Cognitive Science, Palo Alto, CA, November 1997.
251. B. L. Bhuva, V. Janapaty, N. Bui, and S. E. Kerns, "Plasma-induced polarity dependent hot-carrier response of CMOS devices across a wafer," Presented at the 1997 IEEE International Reliability Workshop, Lake Tahoe, NV, November 1997.
252. V. Janapaty, B. L. Bhuva, N. Bui, and S. E. Kerns, "Coupling between hot-carrier degradations modes of pMOSFETs," Presented at the 1997 International Conference on Microelectronic Manufacturing Yield, Reliability, and Failure Analysis, Austin, TX, October 1997.

253. B. L. Bhuva, V. Janapaty, N. Bui, and S. E. Kerns, "Statistical effects of plasma-etch damage on hot-carrier degradation," Presented at the 1997 International Conference on Microelectronic Manufacturing Yield, Reliability, and Failure Analysis, Austin, TX, October 1997.
254. S. E. Kerns, P. Karhade, B. L. Bhuva, and D. V. Kerns, Jr., "Method for evaluating suitability of COTS devices for use in radiation environments," Presented at the 1997 European Conference on Radiation and Its Effects on Components and Systems, Cannes, France, August 1997.
255. B. L. Bhuva, V. Janapaty, N. Bui, and S. E. Kerns, "A study of plasma-induced charging damage using various carrier-injection conditions and time-expanded waveform approach," Presented at the 1997 IEEE International Conference on Plasma Process Induced Damage, Monterey, CA, May 1997.
256. L. W. Massengill, M. Reza, B. L. Bhuva, and T. Turflinger, "Upset cross-section modeling in combinational CMOS logic circuits," Presented at the 1997 Hardened Electronics and Technology Conference, Las Vegas, NV, March 1997.
257. P. Karhade, M. Pagey, B. L. Bhuva, and S. E. Kerns, "StaRS: A tool for statistical reliability simulation of ICs," Presented at the 1996 Semiconductor Research Corporation Technical Conference, Phoenix, AZ, September 1996.
258. M. Satagopan, M. Pagey, B. L. Bhuva, and S. Kerns, "Effects of process variations on device performance and degradations," Presented at the 1996 IEEE Conference on Nuclear and Space Radiation Effects Conference, Indian Wells, CA, July 1996.
259. M. Pagey, R. Milanowski, K. Henegar, B. L. Bhuva, and S. Kerns, "Effects of forming gas, nitrogen, and vacuum anneal effects on X-ray irradiated MOSFET's," Presented at the 1995 IEEE Conference on Nuclear and Space Radiation Effects, Madison, WI, July 1995.
260. W. P. Kang, J. L. Davidson, M. Howel, B. L. Bhuva, D. L. Kinser, D. V. Kerns, Q. Li, and J. F. Xu, "Micro-patterned polycrystalline diamond film emitter array," Presented at the 1995 International Vacuum Microelectronics Conference, Portland, OR, July, 1995.
261. B. L. Bhuva, "StaRS: A simulator for predicting radiation response of ICs in total dose environments," Presented at the Radiation Hardness Assurance Meeting, Dayton, OH, 1994.
262. B. L. Bhuva, L. W. Massengill, and S. E. Kerns, "Vulnerability estimation of SEU uits on complex synchronous systems," Presented at the The 1994 Single-Event Effects Symposium, Manhattan Beach, CA, April 1994.
263. B. L. Bhuva, L. W. Massengill, and S. E. Kerns, "A method for isolation of the effects of SEU hits on latches and combinational circuits," Presented at the The 1994 Single-Event Effects Symposium, Manhattan Beach, CA, April 1994.
264. A. Brown and B. L. Bhuva, "Modeling of charge collection through the ion-shunt fffect in multi-junction structures," Presented at the 1993 IEEE Conference on Nuclear and Radiation Effects, Snowbird, Utah, July 1993.
265. M. P. Pagey, M. H. Yaktieen, A. I. Matta, R. J. Milanowski, B. L. Bhuva, and S. E. Kerns, "Characterization of gate-oxide defects in X-irradiated MOS devices," Presented at the 1993 IEEE Conference on Nuclear and Radiation Effects, Snowbird, Utah, July 1993.
266. N. Kaul, B. L. Bhuva, and S. E. Kerns, "Circuit simulation techniques for single event transients in combinational circuits," Presented at The 1991 IEEE Conference on Nuclear and Space Radiation Effects, San Diego, CA, July 1991.
267. B. L. Bhuva, "The PARA project," Presented at the The Radiation Hardness Assurance Meeting, New Orleans, LA, March 1991
268. C. J. Kee, N. Kaul, G. Biswas, B. L. Bhuva, and J. Vargas, "A student modeling system for ITCDD: An intelligent tutor for CMOS digital design," Presented at the 23rd Southeastern Symposium on System Theory, Columbia, SC, 1991.
269. N. Kaul, B. L. Bhuva, and S. E. Kerns, "Worst case operating frequency determination of CMOS digital VLSI circuits operating in hostile environments," Presented at the 22nd Southeastern Symposium on System Theory, Cookeville, TN, 1990.
270. N. Kaul, B. L. Bhuva, V. Rangavajjhala, H. van der Molen, and S. E. Kerns, "Topology dependent failure exposure levels for CMOS ICs," Presented at the 1990 IEEE Conference on Nuclear and Space Radiation Effects, Reno, NV, July 1990.
271. B. L. Bhuva, S. Mehrotra, L. W. Massengill, and S. E. Kerns, "Dose-rate current partitioning and simulation for CMOS ICs," Presented at the 1990 IEEE Conference on Nuclear and Space Radiation Effects, Reno, NV, July 1990.

272. N. Kaul, B. L. Bhuva, and S. E. Kerns, “Performance analysis of CMOS digital circuits in total dose environments,” Presented at the 1989 IEEE Southeast Conference, Columbia, SC, April 1989.
273. B. L. Bhuva and S. E. Kerns, “Radiation Hardness assurance for Total Dose Environments,” Presented at the 1988 VHSIC/VLSI Qualification, Reliability and Logistics Workshop, Scottsdale, AZ, September 1988.
274. B. L. Bhuva and S. E. Kerns, “Predictive failure simulations for total dose environments,” Presented at the workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance, Hawthorne, CA, April 1988.
275. B. L. Bhuva, J. J. Paulos, R. S. Gyurcsik, S. E. Diehl, and J. H. Moreadith, “Failure mechanisms introduced by statistical variations in CMOS device parameters due to total dose exposure,” Presented at the 1987 IEEE Conference on Nuclear and Space Radiation Effects, Snowmass, CO, July 1987.
276. B. L. Bhuva, R. L. Johnson, Jr., W. J. Stapor, A. B. Campbell, K. W. Fernald, M. A. Xapsos, and S. E. Diehl, “Single-event upsets in a total dose environment: A quantification of the imprint effect,” Presented at the 1987 IEEE Conference on Nuclear and Space Radiation Effects, Snowmass, CO, July, 1987.
277. R. S. Gyurcsik, B. L. Bhuva, and S. E. Diehl, “Automated transistor sizing of CMOS VLSI circuits accounting for total dose radiation effects,” Presented at the 1987 IEEE Conference on Nuclear and Space Radiation Effects, Snowmass, CO, July, 1987.
278. B. L. Bhuva, J. J. Paulos, S. E. Diehl, J. H. Moreadith, S. N. Hong, and R. W. Waltman, “Statistical parameter distribution in total dose environments,” Presented at the 1987 Natural Space Radiation and VLSI Technology Conference, Houston, TX, January, 1987.
279. B. L. Bhuva, J. J. Paulos, and S. E. Diehl, "Circuit simulation of total dose effects,” Presented at the 1986 IEEE Conference on Nuclear and Space Radiation Effects, Providence, RI, July, 1986.
280. W. J. Stapor, A. B. Campbell, M. A. Xapsos, R. L. Johnson, Jr., K. W. Fernald, B. L. Bhuva, and S. E. Diehl, “Single-event upset temperature dependence on MOS static RAMs,” Presented at the 1986 IEEE Conference on Nuclear and Space Radiation Effects, Providence, RI, July, 1986.

External Seminars

Invited Talks and seminars on research projects carried out by Dr. Bhuva’s research group have been presented multiple times at AMD, Cisco, Altera, University of Hong Kong, NetLogic, Avago, LSI Logic, Broadcom, Marvell, DEC, Harris Semiconductor, Hamamatsu, HP, IBM, Intel, Lucent Technologies, National Semiconductor, University of Northern Taiwan Qualcomm, RPI, Texas Instruments, TSMC, UMC, and Xilinx. Dr. Bhuva has also given invited presentations at IEEE International Symposium on Reliability Physics and IEEE International Conference on Integrated Circuits and Device Technologies. Dr. Bhuva has given tutorials at IEEE International Symposium on Reliability Physics.

Book Chapters:

1. Bharat Bhuva and Sherra Kerns, “Plasma-Process-Induced Damage,,” Journal of Science and Technology, Elsevier Science Limited, 14 pages, July 1999.

2. D. L. Schwartz, G. Biswas, J. D. Bransford, B. L. Bhuva**,** T. Balac, and S. Brophy, “Computer Environments for Assessing Learning,” S. Lajoie (Ed.), Computers as Cognitive Tools, Volume II, No More Walls: Theory Change, Paradigm Shifts and Their Influence on the Use of Computers for Instructional Purposes, pp. 273-307, Mahwah, NJ: Erlbaum, 2003.

3. B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, W. T. Holman, A. F. Witulski, “Autonomous Detection and Characterization of Radiation-Induced Transients in Semiconductor Integrated Circuits,” Submitted Book Chapter.

Software Development:

1. **PARA:** software developed for assessing the effects of total dose radiation on circuit parameters. The software identified the dominant failure mechanism caused by shifts in individual device parameters using switch-level algorithms. This was the first tool that showed that failure mechanisms and failure probabilities are circuit design dependent for total dose radiation exposure.

2. **SEUTool**: software developed for evaluating soft error vulnerability of CMOS digital circuits. This was the first software that identified various probabilities for soft error generation and propagation. Algorithms developed for this tool are being used by everyone in the industry.

Graduate Student Advising

1. Nelson Gaspard, Ph.D. student, Single-Event Upset Technology Scaling Trends of Unhardened and Hardened Flip-Flops in Bulk CMOS, Graduation expected May 2015, Supported by Soft Error Consortium.
2. Thiago Assis, Ph.D. student, Primary advisor. Student is supported by funds from industry coalition for soft error research. Graduation expected May 2015, Supported by Soft Error Consortium.
3. Hui Jiang, "*Drosophila* automated olfactory training and testing system for associative learning," Student was supported by research funds from Bioscience and EECS departments, December 2014, Supported by EECS Department and BioScience Department.
4. Nihaar Mahatme, Ph.D. student, Soft Errors Reliability Aware Low Power Design, July 2014, Supported by Soft Error Consortium.
5. Indranil Chatterjee, Ph.D. student, Process Parameters affecting the Total Ionizing Dose Response of FDSOI Planar, Bulk and SOI FinFETs and FDSOI FinFETs, July 2014, Supported by Soft Error Consortium.
6. Zachary Diggins, "Using capacitance to radiation-harden flip-flops at advanced technology nodes," August 2013. The student was supported on a grant from DTRA.
7. Luonan Wang, M.S. The student was supported by a teaching assistantship from EECS department.
8. Amy Kauppila, Analysis of Parameter Variation Impact of the Single Event Response in Sub-100 nm CMOS Storage Cells, April 2012, Supported by EECS Department and Cisco Systems, Inc.
9. Adeola Adekele, Logic Repair and Soft Error Rate Reduction Using Approximate Logic Functions, May 2012, Supported by Cisco Systems, Inc.
10. Indranil Chatterjee, Single-Event Charge Collection and Upsets in 40-nm Dual- and Triple-well Bulk CMOS SRAMs, March 2012, Supported by Cisco Systems, Inc.
11. Lakshmi Tekumula, On-Chip Characterization of Single-Event Charge Collection Process, July 2012, Supported by EECS Department and Cisco Systems, Inc.Edward Ossi, Soft-Error Mitigation at the Architecture-Level Using Berger Codes for Error Detection, December 2011. Supported by grants from Cisco Systems.
12. Nihaar Mahatme, Comparison of Combinational and Sequential Error Rates and Low Overhead Technique for SET mitigation, December 2011. Supported by grants from Cisco Systems.
13. Matthew Gadlage , Impact of temperature on single-event transients in deep submicron bulk and Silicon-on-insulator digital technologies, May 2010. Student was supported by funds from Nav-Sea, Crane, IN.
14. Vijay Sheshadri, Upset trends in flip-flop designs at deep submicron technologies, May 2010. Supported by grants from Cisco Systems.
15. Ryan Bickham, An analysis of error detection techniques for arithmetic logic units, May 2010. Supported by EECS and by grants from Cisco Systems.
16. Corey Toomey, Statistical fault injection and analysis at the regiaster transfer level using the Verilog procedural interface, December 2010. Supported by grants from Cisco Systems.
17. Megan Casey, Ph.D., Single-event effects in digital CMOS circuits operating at ultra-low power, September 2009
18. Balaji Narasimham, Ph.D., Characterization of heavy-ion, neutron, and alpha particle-induced single-event transient pulse widths in advanced technologies, 2008 (Employment with Broadcom, Irvine, CA)
19. Anupama Balasubramanian, Ph.D., Measurement and analysis of single-event induced crosstalk in nanoscale CMOS technologies, 2008 (Employment with Intel, Beaverton, OR)

20. Anitha Balasubramanian, M.S., A built-in self-test (BIST) technique for hardness assurance against SETs in digital circuits, 2008
21. Christopher Holt, M.S., Co-advisor, Analysis of single event transients in dynamic logic circuitry, 2008
22. Patrick Fleming, M.S., An RHBD approach to improve the single-event vulnerability of differential circuits, 2007 (Employment with BAE Systems, Bethesda, MD)
23. Megan Casey, M.S., Cascode-voltage switch logic family of gates for single-event tolerant digital designs, 2006
24. Balaji Narasimham, M.S., On chip characterization of single event transient pulse widths, 2005 (Employment with Broadcom, Irvine, CA)
25. Anupama Balasubramanian, M.S., A silicon based capacitive sensor and analysis circuit for virus detection, 2004 (Employment with Intel, Beaverton, OR)
26. Saurabh Kumar, M.S., Development of DNA hybridization detection on a silicon chip, 2003 (Employed by Dell Computers, Austin, TX)
27. Amit Verma, M.S., All Si-based optical interconnect for signal transmission and optical wave-guide fabrication, 2002 (Assistant Professor of EE, Texas A&M University, Kingsville, TX)
28. Manish Pagey, M.S. Co-advisor, Characterization and modeling of hot-carrier degradation in sub-micron nMOSFETs, 2002 (Employed by L-3 Communications, San Diego, CA)
29. Chen Chen, M.S., DNA hybridization detection using integrated circuits on a silicon chip, 2001
30. Dong Jiang, M.S., Light emission from silicon p-n junctions in avalanche breakdown for use in optical interconnect systems, 2000
31. Pitsini Mongkolkachit, M.S., Evaluation of device lifetime due to hot-carrier effects under dynamic stress, 1999
32. Prashant Karhade, M.S., StaRS : a tool for statistical reliability simulation of ICs, 1997
33. Vijay Janapati, M.S., Characterization of plasma process-induced damage of gate oxide using hot-carrier stressing experiments, 1997 (Senior Marketing Manager at LSI Logic Corporation, Milpitas, CA)
34. Anju Kaul, M.S., Statistical switch-level simulator for advanced VLSI circuits, 1995 **(**Director of Engineering at FunMobility, San Francisco, CA)
35. Murlidharan Satagopan, M.S., Evaluation of single event vulnerability for complex digital circuits, 1994 (Employed by Microsoft, Redmond, WA)
36. Paul Benson, M.S., A new approach for the performance analysis of CMOS digital ICS under device parameter shifts, 1993 (Development Manager at Dell, Austin, TX)
37. Neeraj Kaul, Ph.D., Computer-aided estimation of vulnerability of CMOS VLSI circuits to single-event upsets, 1992 (R&D Group Director at Synopsys Inc.)
38. Sharad Mehrotra, M.S., Test vector generation for critical path sensitization in CMOS circuits, 1991 (Vice-President of Engineering at Pysix Technology, Austin, TX)
39. Chang Jin Kee, M.S., A student modeling system for ITCDD : an intelligent tutor for CMOS digital design, 1990
40. Ishwardutt Parulkar, M.S., A look-up table simulator for transient analysis of BiCMOS circuits, 1990 (Distinguished Engineer at Sun Microsystems, Palo Alto, CA)
41. V. Rangavajjhala, M.S., Infant failure analysis of digital CMOS ICs, 1990 **(**Staff Engineer at Juniper Networks, Milpitas, CA)
42. Neeraj Kaul, M.S., Performance analysis of CMOS digital ICs under device parameter shifts, 1989 (R&D Group Director at Synopsys Inc.)
43. Chanchai Neerapattanagul, M.S.
44. Ahmad Al-Johani, M.S.
45. Mustafa Oner, M.S.

Courses Taught, Developed, and/or Significantly Revised:

ES 140, Introduction to Engineering, Fall 2004
EECE 112, Electrical Engineering Science, Spring 1989
EECE 116, Digital Logic

EECE 216, Electronic Engineering I
EECE 275, Advanced Digital Circuits and Microprocessors I
EECE 277, FPGA Design
EECE 285, VLSI Design
EECE 280, Advanced Electronics II
EECE 306, Introduction to Solid State Materials
EECE 341, Analog Circuits
EECE 395, Design Automation
EECE 396, VLSI Design and Manufacturing Processes

Undergraduate Research:

Most undergraduate research projects were either in support of graduate-level projects or were exploratory projects that later turned into graduate-level projects. The total number of undergraduate project supervised is more than 25. Most of these undergraduate students went on to graduate school.

Professional Service:

Conference Organization Committees

Workshop Organizer for IEEE/ACM Frontiers in Education Conference; 1993
Member of the Technical Committee for IEEE International Reliability Physics Symposium; 1998, 1999, 2000, 2010
Member of Technical Program Committee for IEEE International Reliability Workshop; 1999
Session Chair for IEEE Nuclear and Space Radiation Effects Conference; 2006
Session Chair for RADECS 2009
Member of the Technical Committee for IEEE NUiCone 2013
Member of the Technical Committee for IEEE International Symposium on VLSI Design and Test 2015

Proposal Reviewing

Reviewer for various programs at NSF continuously since 2001

Journal and Conference Reviewing

Design Automation Conference
Circuits and Systems Conference
IEEE Regional Conferences
The International Journal of Electrical and Computer Engineering
IEEE Nuclear and Space Radiation Effects Conference
IEEE Journal of Solid-State Circuits
IEEE Trans. Nucl. Sci.
IEEE Electron Device Letters
IEEE Trans. Electron Devices
IEEE Trans. VLSI Systems
IEEE Trans. On Circuits and Systems

IEEE International Symposium on Circuits and Systems
International Journal of Electronic Testing
European Radiation Effects Conference
IEEE/OSA Journal of Lightwave Technology
Elsevier Microelectronics journal
Journal of Selected Topics in Quantum Electronics

Academic Service:

University

Graduate Faculty Council 2006-Present (Vice-Chair 2008 - 2009)
Provost's Committee for Upperclassmen Experience (2008 – Present)
Vanderbilt Commons Faculty Associate (2008 - Present)
Vanderbilt Visions (2007 – Present),
Vanderbilt Community Giving Campaign (2007)
Parking Committee (2004 – 2006)
Provost' Committee for Student Recreation Center (2002 – 2004)
Graduate Faculty Delegate Assembly (1994 – 2000)
University Research Council (1995 – 1996)
Student Project Fund committee (1989 – 1991)

School of Engineering

Admissions and Scholarship committee (2005 – Present)
Graduate Committee (2008 – 2012)
Library committee (1994 – 1999)
Up-Front committee (1992 – 1994)
Freshmen Recruiting Committee (1990)

Department of EECS

Director of Graduate Studies (2008 – 2013)
Faculty Advisor to Eta Kappa Nu Honor Society (1989 – 2013)
Engage Mentor for Computer Engineering majors (2006 - Present)
EE Academic Advisor to the Class of 2006
Ad-Hoc Computer Engineering Committee (2006)
EE Academic Advisor to the Class of 2002
Graduate Program and Curriculum Committee (Chair 1989 - 1993, 1994 -2001)
EE Academic Advisor to the Class of 1999
Computer Engineering Program committee (1991 – 2001)
EE Academic Advisor to the Class of 1995
Curriculum Reduction and Improvement Committee (Chair, 1992 - 1994)
EE Academic Advisor to the Class of 1992
Graduate Studies committee (1988)

Other Activities:

Coach for Destination Imagination team 2006, 2008 (competed at the Global tournament)

Co-founded seven different startup companies specializing in operations ranging from manufacturing of portable audio/video equipment to retail food sales.